IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a plurality of first standard cells that form a cell array, each of the first standard cells having no contact pattern;

a second standard cell that forms the cell array in combination with the first standard cells, the second standard cell having first contact patterns; and

second contact patterns placed within the cell array and at least between the first standard cells, the number of the second contact patterns being smaller than ~~that~~ the number of the first standard cells.

2. (Currently Amended) The device according to claim 1, wherein the second contact patterns are placed and distributed uniformly within the cell array.

3. (Original) The device according to claim 1, further comprising a well region to which the second contact patterns are connected.

4. (Original) The device according to claim 3, wherein the second contact patterns are placed in positions in the cell array where current density is distributed uniformly.

5. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~according to claim 1~~ comprising:

a plurality of first standard cells that form a cell array, each of the first standard cells having no contact pattern;

a second standard cell that forms the cell array in combination with the first standard cells, the second standard cell having first contact patterns; and

second contact patterns placed within the cell array, the number of the second contact patterns being smaller than the number of the first standard cells,

wherein each of the first standard cells includes a first pattern of active regions of a first MOS transistor of a second conductivity type formed on a well region of a first conductivity type, a second pattern of active regions of a second MOS transistor of the first conductivity type formed on a well region of the second conductivity type, and a first gate interconnection pattern placed in common with the first and second patterns.

6. (Currently Amended) ~~The~~ A semiconductor integrated circuit device ~~according to claim 1~~ comprising:

a plurality of first standard cells that form a cell array, each of the first standard cells having no contact pattern;

a second standard cell that forms the cell array in combination with the first standard cells, the second standard cell having first contact patterns; and

second contact patterns placed within the cell array, the number of the second contact patterns being smaller than the number of the first standard cells,

wherein the second standard cell includes third and fourth patterns of active regions of third and fourth MOS transistors of a second conductivity type formed on a well region of a first conductivity type, fifth and sixth patterns of active regions of fifth and sixth MOS transistors of the first conductivity type formed on a well region of the second conductivity type, a second gate interconnection pattern placed in common with the third and fifth patterns, a third gate interconnection pattern placed in common with the fourth and sixth patterns, third contact pattern as the first contact patterns placed between the third and fourth

pattern, and fourth contact pattern as the first contact patterns placed between the fifth and sixth standard cells, respectively.

7. (Original) A semiconductor integrated circuit device comprising:

a first well region of a first conductivity type;

a second well region of a second conductivity type placed adjacent to the first well region;

a plurality of first standard cells that form a cell array, each of the first standard cells comprising:

a first pattern of active regions of a first MOS transistor of the second conductivity type formed on the first well region;

a second pattern of active regions of a second MOS transistor of the first conductivity type formed on the second well region; and

a first gate interconnection pattern placed in common with the first and second patterns,

the first standard cells having no contact pattern;

a second standard cell that forms the cell array in combination with the first standard cells, each of the second standard cells including:

third and fourth patterns of active regions of third and fourth MOS transistors of a second conductivity type formed on the first well region;

fifth and sixth patterns of active regions of fifth and sixth MOS transistors of the first conductivity type formed on the second well region;

a second gate interconnection pattern placed in common with the third and fifth

patterns;

a third gate interconnection pattern placed in common with the fourth and sixth patterns;

a first contact pattern placed between the third and fourth patterns, the first contact pattern being connected to the first well region;

a second contact pattern placed between the fifth and sixth patterns, the second contact pattern being connected to the second well region;

third and fourth contact patterns placed within the cell array, the third and fourth contact patterns being connected to the first and second well regions, respectively, the third contact patterns being less in number than the first patterns, and fourth contact patterns being less in number than the second patterns.

8. (Original) The device according to claim 7, further comprising a first power supply interconnection placed in a straight line over the first well region, the first power supply interconnection being connected to the first and third contact patterns; and

a second power supply interconnection placed in a straight line over the second well region, the second power supply interconnection being connected to the second and fourth contact patterns.